AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (Currently Amended) An asynchronous transfer mode (ATM) cell switching method, comprising:

a) dividing an input ATM adaptation layer 2 (AAL2) cell into AAL2 type common part sublayer (CPS) packets;

b) sequentially storing the divided CPS packets into first storage areas ~~in accordance~~ with each first storage area corresponding to a different one of a plurality of virtual paths/virtual channels (VPs/VCs) of the respective CPS packets, and sequentially storing first identifiers of the first storage areas, each first identifier corresponding to a different one of the first storage areas and to a different one of the plurality of VPs/VCs, wherein the sequentially storing the first identifiers includes generating a first reference table that maps each of the first identifiers to the corresponding one of the VPs/VCs;

c) reading the stored CPS packets in the order of the stored first identifiers, sequentially storing the read CPS packets in second storage areas used to route the CPS packets to each destination, ~~in accordance with respective~~ wherein each second storage area corresponds to a different one of a plurality of destination channel identifiers (CIDs), and sequentially storing second identifiers of the second storage areas, each second identifier corresponding to a different one of the second storage areas and to a different one of the plurality of destination CIDs, wherein the sequential storing the second identifiers includes generating a second

reference table that maps each of the second identifiers to the corresponding one of the plurality of destination CIDs; and

d) reading the CPS packets, in the order of the second identifiers, from the second storage areas and multiplexing the read CPS packets to generate a reconstructed AAL2 cell,

wherein c) comprises changing origination CIDs of the read CPS packets to the corresponding destination CIDs, and sequentially storing the read CPS packets in the second storage areas corresponding to the destination CIDs.

2. (Canceled)

3. (Original) The ATM cell switching method of claim 1, wherein the CPS packets are stored in the first and second storage areas according to their respective order of arrival.

4. (Original) The ATM cell switching method of claim 1, wherein the CPS packets are read from the first and second storage areas according to their respective order of storage.

5-6. (Canceled)

7. (Previously Presented) The ATM cell switching method of claim 1, wherein the first and second identifiers are stored in the order that the CPS packets are stored to the corresponding first and second storage areas, respectively.

8. (Previously Presented) The ATM cell switching method of claim 1, wherein the CPS packets are read from the first and second storage areas according to their respective order of storage.

9. (Previously Presented) The ATM cell switching method of claim 1, further comprising implementing a switching test by reading the CPS packets from the second storage areas in the order of the second identifiers and comparing the read CPS packets to a standard.

10. (Previously Presented) The ATM cell switching method of claim 1, further comprising implementing a switch signaling by reading the CPS packets from the second storage areas in the order of the second identifiers and outputting the read CPS packets to a processor.

11. (Previously Presented) The ATM cell switching method of claim 1, further comprising routing the CPS packets stored in the first storage areas to another switch in the order of the first identifiers.

12. (Previously Presented) The ATM cell switching method of claim 1, wherein the first and second storage areas each have a queue type structure.

13. (Canceled)

14. (Currently Amended) An asynchronous transfer mode (ATM) cell switching system, comprising:

a reassembly processing unit that divides an input ATM adaptation layer 2 (AAL2) cell into AAL2-type common part sublayer (CPS) packets;

a first memory that sequentially stores the divided CPS packets into first storage areas with each first storage area corresponding to a different one of a plurality of virtual paths/virtual channels (VPs/VCs) and that sequentially stores first identifiers of the first storage areas, each first identifier corresponding to a different one of the first storage areas and to a different one of the plurality of VPs/VCs, wherein the first memory includes a first reference table that maps the first identifiers to the corresponding one of the plurality of VPs/VCs;

a CPS packet switching unit that reads the stored CPS packets from the first storage areas in an order of the stored first identifiers and routes the read CPS packets to each destination;

a second memory that sequentially stores the routed CPS packets into second storage areas with each second storage area corresponding to a different one of a plurality of destination channel identifiers (CIDs), and sequentially stores second identifiers of the second storage areas, each second identifier corresponding to a different one of the second storage areas and to a different one of the plurality of destination CIDs, wherein the second memory includes a second reference table that maps the second identifiers to the corresponding one of the plurality of destination CIDs; and

an assembly processing unit that reads the CPS packets from the second storage areas in an order of the second identifiers and multiplexes the CPS packets read from the second storage areas to generate a reconstructed AAL2 cell,

wherein the CPS packet switching unit changes origination channel identifiers (CIDs) of the CPS packets read from the first storage areas to the corresponding destination CIDs and sequentially stores the read CPS packets in the second storage areas corresponding to the destination CIDs.

15. (Canceled)

16. (Currently Amended) An asynchronous transfer mode (ATM) cell switching system, comprising:

first, second, third, and fourth memories that sequentially store ATM adaptation layer 2 (AAL2) type common part sublayer (CPS) packets and output the CPS packets in the order of their respective storage, wherein each memory has a plurality of storage areas;

a reassembly processing unit that divides an input AAL2 cell into the AAL2 type CPS packets, stores the divided CPS packets in different first storage areas of the first memory ~~in accordance~~ with each first storage area corresponding to a different one of a plurality of virtual paths/virtual channels (VPs/VCs), and stores first identifiers of the different first storage areas in the second memory, each first storage area having a different first identifier that corresponds to one of the plurality of VPs/VCs;

a CPS packet switching unit that reads the CPS packets stored in the first memory in an order of the first identifiers stored in the second memory, stores the read CPS packets in different second storage areas of the third memory ~~in accordance~~ with each second storage area corresponding to a different one of a plurality of destination channel identifiers (CIDs), and stores second identifiers of the second storage areas in the fourth memory, each second storage area having a different second identifier that corresponds to one of the plurality of destination CIDs; and

an assembly processing unit that reads the CPS packets stored in the third memory in an order of the second identifiers stored in the fourth memory and multiplexes the read CPS packets to generate a reconstructed AAL2 cell.

17. (Original) The ATM cell switching system of claim 16, further comprising:

a first reference table that maps the first identifiers with the corresponding VPs/VCs; and

a second reference table that maps the second identifiers with the corresponding destination CIDs.

18. (Original) The ATM cell switching system of claim 17, wherein the reassembly processing unit refers to the first reference table to determine the first storage areas corresponding to the VPs/VCs of the CPS packets.

19. (Original) The ATM cell switching system of claim 17, wherein the CPS packet switching unit refers to the second reference table to determine the respective destination CIDs corresponding to the CPS packets.

20. (Original) The ATM cell switching system of claim 19, wherein the CPS packet switching unit changes origination CIDs of the CPS packets read from the first memory to the corresponding destination CIDs, with reference to the second reference table.

21. (Original) The ATM cell switching system of claim 16, wherein the first and second identifiers are stored in the order that the CPS packets are stored to the corresponding first and second storage areas, respectively.

22. (Previously Presented) The ATM cell switching system of claim 16, wherein the first, second, third, and fourth memories each have a queue type structure.

23. (Original) The ATM cell switching system of claim 16, further comprising:

a central processing unit that reads the CPS packets from the first memory in the order of the stored first identifiers and implements testing and signaling for switching.

24. (Previously Presented) The ATM cell switching system of claim 23, wherein the first, second, third, and fourth memories each have a queue type structure.

25. (Previously Presented) The ATM cell switching system of claim 16, further comprising:

a plurality of cell switches that each has first, second, third, and fourth memories, a reassembly processing unit, a CPS packet switching unit, and an assembly processing unit; and

a router that routes the CPS packets output from one of the plurality of cell switches to another cell switch.

26. (Previously Presented) The cell switching system of claim 25, wherein the first, second, third, and fourth memories each have a queue type structure.

27-28. (Canceled)